Claims

1. A method for storing data in a magnetoresistive solid-state storage device having an array of storage cells, the method comprising the steps of:

encoding a logical unit of original information to form a block of ECC encoded data; and

storing the block of ECC encoded data in the array of storage cells.

2. The method of claim 1, wherein the storage cells of the array are arranged in rows, wherein the ECC encoded data is formed having multi-bit symbols, and wherein a plurality of bits from a multi-bit symbol are stored in one of the rows.

3. The method of claim 1, wherein the storage cells of the array are arranged in rows, and all bits of a multi-bit symbol are stored in a single row.

4. The method of claim 2, wherein the block of ECC encoded data comprises a plurality of n-bit symbols, with all n bits of each symbol being stored in one row of the rows of storage cells.

5. The method of claim 4, wherein the n bits of a symbol are spaced at least a minimum reading distance m apart, such that all n bits are readable from a row in a single slice.

6. The method of claim 1, wherein the storage device comprises plural arrays, at least some of the arrays being arranged to store one or more symbols of the block of ECC encoded data.

7. The method of claim 6, wherein each of the plural arrays is arranged to store one or more symbols of the block of ECC encoded data.

8. The method of claim 6, wherein at least a substantial portion of the block of ECC encoded data is readable from the device in a single slice.

9. The method of claim 8, wherein the slice comprises accessing one row from each of the plural arrays.

10. The method of claim 1, wherein the storage cells of the array are arranged in rows, wherein the ECC encoded data is formed having multi-bit symbols, and wherein a multi-bit symbol is stored with one or more bits in at least two of the rows.

11. The method of claim 10, wherein for each multi-bit symbol a first set of bits are stored in a first row, and a second set of bits are stored in a second row, such that at least some columns of the first set of bits are common to at least some columns of the second set of bits.

12. The method of claim 11, wherein each of the first and second sets of bits comprises a plurality of bits.

13. The method of claim 11, wherein each n-bit symbol is stored across a plurality of rows r, and the n bits of

each symbol are stored in an arrangement of storage cells according to r x (n/r).

14. The method of claim 10, wherein each symbol is readable by taking a slice from each of the at least two rows.

15. The method of claim 14, wherein the storage device comprises plural arrays, at least some of the plural arrays being arranged to store one or more symbols of the block of ECC encoded data, such that at least a substantial portion of the block of ECC encoded data is readable from the device in a single slice.

16. The method of claim 15, wherein each slice comprises accessing one row from each of the plural arrays.

17. The method of claim 1, wherein the storage cells of the array are arranged in rows, wherein the ECC encoded data is formed having multi-bit symbols, and wherein at least one of the rows stores a set of bits from at least two of the multi-bit symbols.

18. The method of claim 17, wherein each set of bits is allocated to a different one of at least two blocks of ECC encoded data.

19. The method of claim 17, wherein each set of bits is allocated to a different one of a plurality of codewords, plural codewords being associated to form a sector of ECC encoded data representing the logical unit of original information.

20. The method of claim 19, wherein the sets of bits are each allocated to symbols within a different codeword of a single sector of ECC encoded data.

21. The method of claim 17, wherein each of the sets of bits comprises all bits from a multi-bit symbol, such that for each multi-bit symbol all bits are stored in a single row.

22. The method of claim 17, wherein a multi-bit symbol is stored with bits in at least two rows.

23. The method of claim 22, wherein for each multi-bit symbol a first set of bits are stored in a first row, and a second set of bits are stored in a second row, such that at least some columns of the first set of bits are common to at least some columns of the second set of bits.

24. The method of claim 1, wherein the storage cells of the array are arranged in rows, wherein the ECC encoded data is formed having single-bit symbols, and wherein at least one of the rows stores at least two of the single-bit symbols.

25. The method of claim 24, wherein each of the at least two single-bit symbols is allocated to a different one of at least two blocks of encoded data.

26. The method of claim 25, wherein each of the at least two single-bit symbols is allocated to a different one of a plurality of codewords, plural codewords being

associated to form a sector of ECC encoded data representing a logical unit of original information.

27. The method of claim 26, wherein each of the at least two single-bit symbols is allocated to a different codeword of a single sector of ECC encoded data.

28. The method of claim 1, wherein the storage cells are arranged in rows, each row storing a set of bits from each of at least two symbols, the sets of bits in each row being allocated to at least two different units of encoded data, and an order of allocation amongst the units of encoded data being changed between at least some rows.

29. The method of claim 28, wherein a first row stores a set of bits from a symbol allocated to a first codeword, and a set of bits from a symbol allocated to a second codeword, and a second row storing, in order, a set of bits from a symbol allocated to the second codeword, and then a set of bits from a symbol allocated to the first codeword.

30. The method of claim 28, wherein the sets of bits in each row share at least some columns.

31. The method of claim 28, wherein the order of allocation is rotated between at least some rows.

32. The method of claim 1, wherein the ECC encoded data is formed having multi-bit symbols, and wherein the encoding step comprises forming an error check for each multi-bit symbol.

33. The method of claim 32, comprising providing at least one error detecting bit associated with each multi-bit symbol.

34. The method of claim 33, wherein the error detecting bit or bits allow a parity check to be performed on the multi-bit symbol.

35. The method of claim 33, wherein the storing step comprises storing each multi-bit symbol and one or more error detecting bits together in the array as a symbol unit.

36. The method of claim 35, wherein the storing step comprises storing each symbol unit with all bits in a single row of storage cells.

37. The method of claim 35, wherein the storing step comprises storing each symbol unit with bits in at least two rows of storage cells.

38. The method of claim 37, wherein the storage cells are arranged in rows and columns and, for a symbol unit, a first set of bits are stored in a first row, and a second set of bits are stored in a second row, such that at least some columns of the first set of bits are common to at least some columns of the second set of bits.

39. A magnetoresistive solid-state storage device, comprising:

at least one array of magnetoresistive storage cells;

an ECC encoding unit for encoding a logical unit of original information to form a block of ECC encoded data; and

a controller for storing the block of ECC encoded data in the at least one array of storage cells.

40. The device of claim 39, wherein the storage cells of the array are arranged in rows, wherein the ECC encoded data is formed having multi-bit symbols, and wherein a plurality of bits from a multi-bit symbol are stored in one of the rows.

41. The device of claim 39, wherein the storage cells of the array are arranged in rows, and all bits of a multi-bit symbol of ECC encoded data are stored in a single row.

42. The device of claim 41, wherein the block of ECC encoded data comprises a plurality of n-bit symbols, with all n bits of each symbol being stored in one row of the rows of storage cells.

43. The device of claim 42, wherein the n bits of a symbol are spaced at least a minimum reading distance m apart, such that all n bits are readable from a row in a single slice.

44. The device of claim 43, wherein the storage device comprises plural arrays, at least some of the arrays being arranged to store one or more symbols of the block of ECC encoded data.

45. The device of claim 44, wherein each of the plural arrays is arranged to store one or more symbols of the block of ECC encoded data.

46. The device of claim 45, wherein at least a substantial portion of the block of ECC encoded data is readable from the device in a single slice.

47. The device of claim 46, wherein the slice comprises accessing one row from each of the plural arrays.

48. The device of claim 39, wherein the storage cells of the array are arranged in rows, wherein the ECC encoded data is formed having multi-bit symbols, and wherein a multi-bit symbol is stored with one or more bits in at least two of the rows.

49. The device of claim 48, wherein for each multi-bit symbol a first set of bits are stored in a first row, and a second set of bits are stored in a second row, such that at least some columns of the first set of bits are common to at least some columns of the second set of bits.

50. The device of claim 49, wherein each of the first and second sets of bits comprises a plurality of bits.

51. The device of claim 49, wherein each n-bit symbol is stored across a plurality of rows r, and the n bits of each symbol are stored in an arrangement of storage cells according to $r \times (n/r)$.

52. The device of claim 48, wherein each symbol is readable by taking a slice from each of the at least two rows.

53. The device of claim 52, wherein the storage device comprises plural arrays, at least some of the plural arrays being arranged to store one or more symbols of the block of ECC encoded data, such that at least a substantial portion of the block of ECC encoded data is readable from the device in a single slice.

54. The device of claim 53, wherein each slice comprises accessing one row from each of the plural arrays.

55. The device of claim 39, wherein the storage cells of the array are arranged in rows, wherein the ECC encoded data is formed having multi-bit symbols, and wherein at least one of the rows stores a set of bits from at least two of the multi-bit symbols.

56. The device of claim 55, wherein each set of bits is allocated to a different one of at least two blocks of encoded data.

57. The device of claim 56, wherein each set of bits is allocated to a different one of a plurality of codewords, plural codewords being associated to form a sector of ECC encoded data representing a logical unit of original information.

58. The device of claim 57, wherein the sets of bits are each allocated to symbols within a different codeword of a single sector of ECC encoded data.

59. The device of claim 55, wherein each of the sets of bits comprises all bits from a multi-bit symbol, such that for each multi-bit symbol all bits are stored in a single row.

60. The device of claim 55, wherein a multi-bit symbol is stored with bits in at least two rows.

61. The device of claim 60, wherein for each multi-bit symbol a first set of bits are stored in a first row, and a second set of bits are stored in a second row, such that at least some columns of the first set of bits are common to at least some columns of the second set of bits.

62. The device of claim 39, wherein the storage cells of the array are arranged in rows, wherein the ECC encoded data is formed having single-bit symbols, and wherein at least one of the rows stores at least two of the single-bit symbols.

63. The device of claim 62, wherein each of the at least two single-bit symbols is allocated to a different one of at least two blocks of encoded data.

64. The device of claim 63, wherein each of the at least two single-bit symbols is allocated to a different one of a plurality of codewords, plural codewords being associated to form a sector of ECC encoded data representing a logical unit of original information.

65. The device of claim 64, wherein the at least two single-bit symbols are each allocated to a different codeword of a single sector of ECC encoded data.

66. The device of claim 39, wherein the storage cells are arranged in rows, each row storing a set of bits from each of at least two symbols, the sets of bits in each row being allocated to at least two different units of encoded data, and an order of allocation amongst the units of encoded data being changed between at least some rows.

67. The device of claim 66, wherein a first row stores a set of bits from a symbol allocated to a first codeword, and a set of bits from a symbol allocated to a second codeword, and a second row storing, in order, a set of bits from a symbol allocated to the second codeword, and then a set of bits from a symbol allocated to the first codeword.

68. The device of claim 66, wherein the sets of bits in a first row share at least some columns with the sets of bits in a second row.

69. The device of claim 66, wherein the order of allocation is rotated between at least some rows.

70. The device of claim 39, wherein the ECC encoded data is formed having multi-bit symbols, and wherein the ECC encoding unit forms an error check for each multi-bit symbol.

71. The device of claim 70, wherein the ECC encoding unit forms at least one error detecting bit associated with each multi-bit symbol.

72. The device of claim 71, wherein the error detecting bit or bits allow a parity check to be performed on the multi-bit symbol.

73. The device of claim 72, wherein each multi-bit symbol and one or more error detecting bits are stored together in the array as a symbol unit.

74. The device of claim 73, wherein each symbol unit is stored having all bits in a single row of storage cells.

75. The device of claim 73, wherein each symbol unit is stored having bits in at least two rows of storage cells.

76. The device of claim 75, wherein the storage cells are arranged in rows and columns and, for a symbol unit, a first set of bits are stored in a first row, and a second set of bits are stored in a second row, such that at least some columns of the first set of bits are common to at least some columns of the second set of bits.

77. An apparatus comprising the magnetoresistive solid-state storage device of claim 39.